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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,912	KIM ET AL.	
	Examiner	Art Unit	
	TAMMY PHAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,8,9,11,12,14-27,29,30 and 32-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8,9,11,12,14-27,29,30 and 32-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 2, 4-7, 10, 13, 28, 31, 33, 35-47, have been cancelled. Independent claims 1, 9, have been amended. Claims 1, 3, 8-9, 11-12, 14-27, 29-30, 32, 34, are pending.

Response to Arguments

2. Applicant's arguments filed 29 September 2008 have been fully considered, as follows:

3. *§ 112 Rejection*

4. Applicant's amendments of 29 September 2008 overcome the prior 112 rejection, hence the previous 112 rejection has been withdrawn.

5. *§ 103 Rejection*

6. **In regards to independent claim 1,** Applicant submits that *"Cairns1 fails to teach 'a first multiplexer (Fig. 4, item 13) part performing a time-division" because Cairns1 [is] silent in performing time-division (Remarks 10)."* This is not persuasive.

7. The term *"time-division"* is broad and hence Cairnes1 continues to read upon the claim limitations. Because Applicant fails to explicitly define exactly how the multiplexers are performed in a time-divisioned fashion, Examiner will take time-division to mean that the multiplexer are not performed all at once, or all at one timing. Rather, the multiplexers divide up their functions through time. In particular, Cairns1 teaches that the multiplexer (Fig. 4, item 13) are able to select m registers at a time (section [0015]).

8. **In regards to independent claim 1,** Applicant submits that *"Cairns1 fails to teach 'wherein the first multiplexer and the de-multiplexer part are controlled by an ODD/EVEN signal which performs the time-division for a horizontal period' (Remarks 10)."* This is not persuasive.

9. First of all, Cairns1 is not cited to teach of this newly amended claim language. Rather, it is Cairns1 in view of the other references that read upon this claim limitation. In particular, Cairns1 teaches of a first multiplexer (Fig. 4, item 13) and a de-multiplexer (Fig. 4, item 14) which are controlled by a signal which performs time-division for a horizontal period (sections [0009, 00024]); but fails to teach that both the first multiplexer and de-multiplexer are controlled by an ODD/EVEN signal which performs time-division for a horizontal period. As analyzed in the previous office action, Morita was brought in to show that the display components may be controlled by ODD/EVEN signal which performs time-division for a horizontal period (column 8, lines 18-22). One benefit of this combination of Morita's ODD/EVEN controlled signals and Cairns1's display is that this simplifies the display components (Morita, column 3, lines 64-1). Hence, Cairns1 in view of Morita reads upon the newly amended claim language.

10. **In regards to independent claim 1,** Applicant submits that *"Cairns1 fails to teach 'a latch part sequentially latching a digital pixel data in response to the sampling signal from the shift register part' (Remarks 10)."* This is not persuasive.

11. Cairns1 teaches of a latch part (Fig. 4, item 11, since a latch is a basically a storage register) sequentially latching a digital pixel data in response to the sampling signal from the

shift register part (Fig. 8, item 25). Hence, Cairns1 continues to read upon the claim limitations as currently claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030653 A1) in view of Cairns et al. ("Cairns2") (US Patent No: 6,268,841 B1), Enami et al (US Patent No: 5,892,493), and Morita (US Patent No.: 6,989,810 B2).

13. **As for independent claim 1,** Cairns1 teaches of a data driving apparatus (Fig. 1, item 2) for a liquid crystal display device (Fig. 1), comprising:

14. a register part (Fig. 4, item 10) sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal;

15. a latch part (Fig. 4, item 11) sequentially latching a digitally pixel data in response to the sampling signal from the register part (Fig. 4, item 10);

16. a first multiplexer (Fig. 4, item 13) part performing a time-division on digital pixel data from the latch part;

17. a digital-analog converter (Fig. 4, item 12) part converting the time-divided digital pixel data from the first multiplexer (Fig. 4, item 13) part to analog pixel signals;

18. a demultiplexer (Fig. 4, item 14) part supplying the analog pixel signals from the digital-analog converter (Fig. 4, item 12) part to a plurality of output channels (section [0015]); and of providing signals for the enable period of a source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal (Fig. 2).

19. Cairns1 fails to teach of an a shift register;

20. output part sampling and holding the analog pixel signals from the demultiplexer output channels,

21. wherein the output part comprises:

22. a sampling part sampling the pixel signals from the demultiplexer output channels;

23. a holding part holding the sampled pixel signals from the sampling part, and

24. an output buffer part for buffering the sampled pixels signals from the holding part, and

25. a second multiplexer part for outputting the sampled pixel signals from the output buffer part in response to a source output enable signal;

26. wherein the device is controlled by an ODD/EVEN signal which performs the time-division for a horizontal period; and

27. that the signals are separately being supplied during the first half of the horizontal period and during the second half of the horizontal period.

28. Cairns1 explicitly teaches of a shift register in another embodiment (Fig. 8).

29. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the shift register of the other embodiment with Cairns since shift registers ensure that all of the flip flop circuits are able to reset to the "zero" logic state before operation (section [0058]).

30. **Cairns2 teaches of an output part** (Fig. 11b) output part sampling and holding the analog pixel signals from the demultiplexer output channels (Fig. 11b, section "output from demultiplexer"),

31. wherein the output part (Fig. 11b) comprises:

32. a sampling part (Fig. 11b, items 47, 49) sampling the pixel signals from the demultiplexer output channels (Fig. 11b, section "output from demultiplexer");

33. a holding part (Fig. 11b, items C1-C2) holding the sampled pixel signals from the sampling part (Fig. 11b, items 47, 49), providing the corresponding data lines (Fig. 11b, item 8) with the pixel signals from the output buffer part (Fig. 11b, item 40);

34. an output buffer part (Fig. 11b, item 40) for buffering the sampled pixels signals from the holding part (Fig. 11b, items C1-C2); and

35. wherein the device is controlled by an ODD/EVEN signal which performs the time-division for a horizontal period (column 8, lines 20-30).

36. It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (Cairns2, column 4, lines 33-35).

37. Cairns1 and Cairns2 fails to teach of a second multiplexer part.

38. **Enami teaches of a second multiplexer part** (Fig. 1, item 38) for outputting the sampled pixel signals from the output buffer part (Fig. 8b, items 40) in response to a source output enable signal.

39. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include a second multiplexer as taught by Enami with the data driver of Cairns1 and the output part of Cairns2 in order to allow the apparatus to perform multiplex driving in which the data voltage is sequentially applied to a number of data lines in each of the data groups (Enami, column 3, lines 49-51).

40. Cairns1, Cairns2, and Enami fails to teach that the signals are separately being supplied during the first half of the horizontal period and during the second half of the horizontal period.

41. **Morita teaches that the signals are separately being supplied** during the first half of the horizontal period (Fig. 8, items t2-t7) and during the second half of the horizontal period(Fig. 8, items t8-t13, column 8, lines 18-28).

42. It would have been obvious to one with ordinary skill in the art at the time the invention was made have the signals be supplied separately as taught by Morita with the data driving apparatus of Cairns1, the output part of Cairns2, and the second multiplexer part of Enami. The benefits of separating supplying the signals in the first and second horizontal period, is that it allows for a more simple data structure (Morita, column 3, lines 67-1).

43. **As for claim 8,** Cairns1 as modified by Cairns2 and Enami teaches that the sampling switches controlled by an ODD/EVEN signal which performs the time-division on a horizontal period (Cairns2, column 1, lines 54-58).

44. Claims 30, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030652 A1) in view of Cairns et al. ("Cairns2") (US Patent No: 6,268,841 B1).

45. **As for independent claim 30,** Cairns1 teaches of a data driving method (Fig. 1, item 2) for a liquid crystal display device (Fig. 1), comprising:

46. performing a time-division on a digital pixel data (Fig. 4, item 13);

47. converting the time-divided digital pixel data into time-divided analog pixel signals (Fig. 4, item 12);

48. supplying the time-divided analog pixel signals to corresponding output channels (section [0015]);

49. providing the corresponding data lines with the held pixel signals for an enable period of an input source output enable signal and a reference voltage of liquid crystal cells for a disable period of the input source output enable signal (section [0057]).

50. Cairns1 fails to teach of sampling and holding the time-divided analog pixel signals received through the output channels and simultaneously supplying the held pixel signals to corresponding data lines.

51. Cairns2 teaches of sampling and holding (Fig. 11b, items 47, 49) the time-divided analog pixel signals received through the output channels and simultaneously supplying the held pixel signals to corresponding data lines (Fig. 11b, item 8).

52. It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (Cairns2, column 4, lines 33-35).

53. **As for claim 34,** Cairns1 teaches that the sampling the pixel signals is controlled by an ODD/EVEN signal performing a time-division on a horizontal period in section [0065].

54. Claims 3, 32, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030652 A1), in view of Cairns et al. ("Cairns2") (US Patent No: 6,268,841 B1) and Nitta et al. (US Patent No: 6,661,402 B1).

55. **As for claim 3,** Cairns1teaches that the digital-analog converter part (Fig. 4, item 12, section [0019]) and a demultiplexer part (Fig. 4, item 14, section [0016]).

56. Cairns1 fails to teach of a second multiplexer part.

57. Cairns2 teaches of a second multiplexer part (Fig. 11b, items 47, 49, column 10, lines 9-12).

58. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the second multiplexer of Cairns2 with the DAC of Cairns1 in order to provide the apparatus with a data line driver where there are more data lines than data line circuits (Cairns2, column 4, lines 21-25).

59. Cairns1 and Cairns2 fails to teach of a positive digital-analog converter converting the digital pixel data to a positive pixel signal; a negative digital-analog converter converting the digital pixel data to a negative pixel signal in accordance with a polarity control signal.

60. Nitta teaches of a positive digital-analog converter (Fig. 2, item 228, column 3, lines 24-26) converting the digital pixel data to a positive pixel signal; a negative digital-analog converter (Fig. 2, item 229, column 3, lines 27-31) converting the digital pixel data to a negative pixel signal in accordance with a polarity control signal (Fig. 2, item 425, column 6, lines 50-53).

61. It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine separate the signals in accordance to their polarity as taught by Nitta with the driving circuitry of Cairns1 and Cairns2 in order to improve the picture quality by providing a more efficient driving method (Nitta, column 1, lines 50-55).

62. **As for claim 32,** Cairns1 and Cairns2 fails to teach of time-divided digital pixel data comprises: converting the time-divided pixel data to a positive analog pixel signal and a negative analog pixel signal; and selecting one of the positive and the negative analog pixel signals in accordance with a polarity control signal.

63. Nitta teaches that the time-divided digital pixel data comprises: converting the time-divided pixel data to a positive analog pixel signal and a negative analog pixel signal; and selecting one of the positive and the negative analog pixel signals in accordance with a polarity control signal (column 3, lines 23-33; column 4, lines 35-30 and Fig. 2).

64. It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine separate the signals in accordance to their polarity as taught by Nitta with the driving circuitry of Cairns1 and Cairns2 in order to improve the picture quality by providing a more efficient driving method (Nitta, column 1, lines 50-55).

65. Claims 9, 14-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030652 A1), in view of Cairns et al. ("Cairns2") (US Patent No: 6,268,841 B1), Enami et al (US Patent No: 5,892,493), Nitta et al. (US Patent No: 6,661,402 B1), and Morita (US Patent No.: 6,989,810 B2).

66. **As for independent claim 9,** Cairns1 teaches of a data driving apparatus (Fig. 1, item 2) for a liquid crystal display device (Fig. 1), comprising:

67. a register part (Fig. 4, item 10) sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal;

68. a latch part (Fig. 4, item 11) sequentially latching a digitally pixel data in response to the sampling signal from the register part (Fig. 4, item 10);

69. a multiplexer part (Fig. 4, item 13) performing a time-division on input digital pixel data for a plurality of data lines;

70. a digital-analog converter part (Fig. 4, item 12) including:

71. a demultiplexer (Fig. 4, item 14) part supplying the analog pixel signals from the digital-analog converter (Fig. 4, item 12) part to a plurality of output channels in section [0015], and of providing signals for the enable period of a source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal (Fig. 2).

72. Cairns1 fails to teach of a shift register;

73. a level shifter part raising a voltage of the time-divided pixel data;

74. an output part outputting simultaneously the time-divided pixel signals from the corresponding demultiplexer output channels to corresponding data lines,

75. wherein the output part comprises:

76. a sampling part sampling the pixel signals supplied through the output channels of the demultiplexer;

77. a holding part holding the sampled pixel signals provided through the sampling part, and

78. a discharging part discharging the pixel signals held in the holding part for a first period to the corresponding data lines for a second period.

79. a positive digital-analog converter converting a plurality of time divided pixel data for the first horizontal period provided through the positive polarity output channel of the multiplexer part into positivel pixel data;

80. and a negative digital-analog converter converting a plurality of time divided pixel data for the first horizontal period provided through the negative polarity output channel of the multiplexer part into the negative pixel data; and

81. that the signals are separately being supplied during the first half of the horizontal period and during the second half of the horizontal period.

82. Cairns1 explicitly teaches of a shift register in another embodiment (Fig. 8).

83. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the shift register of the other embodiment with Cairns since shift registers ensure that all of the flip flop circuits are able to reset to the "zero" logic state before operation (section [0058]).

84. **Cairns2 teaches of an output part** (Fig. 11b) outputting simultaneously the time-divided pixel signals from the corresponding demultiplexer output channels (Fig. 11b, section "output from demultiplexer") to corresponding data lines (Fig. 11b, item 8),

85. wherein the output part (Fig. 11b) comprises:

86. a sampling part (Fig. 11b, items 47, 49) sampling the pixel signals through the output channels of the demultiplexer (Fig. 11b, section "output from demultiplexer");

87. a holding part (Fig. 11b, items C1-C2) holding the sampled pixel signals provided through the sampling part (Fig. 11b, items 47, 49); and

88. a level shifter part (Fig. 11b, item 40) raising a voltage of the time-divided pixel data.

89. It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (Cairns2, column 4, lines 33-35).

90. Cairnes1 and Cairns2 fails to teach of a discharging part discharging the pixel signals held in the holding part for a first period to the corresponding data lines for a second period.

91. **Enami teaches of a discharging part** (Fig. 1, item 38) discharging the pixel signals held in the holding part for a first period to the corresponding data lines (Cairns2, Fig. 11b, item 8) for a second period.

92. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include a discharging part as taught by Enami with the data driver of Cairns1 and the output part of Cairns2. The benefit of this combination is to allow the apparatus to perform multiplex driving in which the data voltage is sequentially applied to a number of data lines in each of the data groups (Enami, column 3, lines 49-51).

93. Cairns1, Cairns2, and Enami, fails to teach of the components of the driving apparatus having selected polarity.

94. **Nitta teaches of the components of the driving apparatus having selected polarity** through a positive polarity output channel and a negative polarity output channel (column 3, lines 23-33, column 4, lines 25-30).

95. It would have been obvious to one with ordinary skill in the art at the time the invention was made to have selected polarity as taught by Nitta with the various components of the driving apparatus of taught by Cairns1, Cairns2, and Enami in order to increase the speed and functionality of the driver (see Nitta: column 1, lines 50-55).

96. Cairns1, Cairns2, Enami, and Nitta fail to teach that the signals are separately being supplied during the first half of the horizontal period and during the second half of the horizontal period.

97. **Morita teaches that the signals are separately being supplied** during the first half of the horizontal period (Fig. 8, items t2-t7) and during the second half of the horizontal period (Fig. 8, items t8-t13, column 8, lines 18-28).

98. a positive digital-analog converter (Fig. 7) converting a plurality of time divided pixel data for the first horizontal period (Fig. 8, items t2-t7) provided through the positive polarity output channel of the multiplexer part into positivel pixel data;

99. and a negative digital-analog converter (Fig. 7) converting a plurality of time divided pixel data for the second horizontal period (Fig. 8, items t8-t13), provided through the negative polarity output channel of the multiplexer part into the negative pixel data (column 8, lines 18-28).

100. It would have been obvious to one with ordinary skill in the art at the time the invention was made have the signals be supplied separate as taught by Morita with the data driving apparatus of Cairns1, the output part of Cairns2, the second multiplexer part of Enami, and the selected polarity of Nitta. The benefits of separating supplying the signals in the first and second horizontal period, is that it allows for a more simple data structure (Morita, column 3, lines 67-1).

101. **As for claim 10,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the digital-analog converter (Cairns1, Fig. 4, item 12) part comprises: a positive digital-analog converter (Cairns1, Fig. 4, item 12) converting the pixel signal provided through the positive output channel of the multiplexer part into a positive pixel signal; and a negative digital-analog converter (Cairns1, Fig. 4, item 12) converting the pixel signal provided through the negative output channel of the multiplexer part into negative pixel signal (Cairns1, section [0015]) (Nitta, column 3, lines 23-33; column 4, lines 35-30).

102. **As for claim 11,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer part (Cairns1, Fig. 4, item 13) comprises:

103. a plurality of positive path switches coupled to input channels for the pixel data and commonly connected to the positive polarity output channel; and

104. a plurality of negative path switches coupled to the input channels for the pixel data, connected to the positive path switches in parallel, and commonly connected to negative polarity output channel (Cairns1, Fig.4, section [0015]) (Nitta, Fig. 2, column 3, lines 23-33; column 4, lines 35-30).

105. **As for claim 12,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the demultiplexer (Cairns1, Fig. 4, item 14) part comprises: a plurality of positive path switches forming a plurality of different positive paths corresponding to the data lines, and commonly connected to a positive digital-analog converter, and a plurality of negative path switches forming a plurality of different negative paths, commonly connected to a negative digital-analog converter (Id.), wherein the negative path switches are connected to the positive path switches in parallel (Cairns1, Fig.4, section [0015]) (Nitta, Fig. 1, column 3, lines 23-33; column 4, lines 35-30).

106. **As for claim 14,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the sampling part (Cairns2, Fig. 11b) and the holding part sample and hold the pixel signals supplied for the next horizontal period through the channel different from that of the pixel signal supplied for the first horizontal period (Cairns2, Fig. 12, each column has at least three sets of buffers).

107. **As for claim 15,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the sampling part (Cairns2, Fig. 11b) has a second demultiplexer (Cairns2, Fig. 3, item 25) part comprising; a plurality of the positive path switches forming a plurality of different positive paths and connected to the output channels of the demultiplexer part (Id.); and a plurality of negative path switches forming a plurality of different negative paths and connected to the output channels of the demultiplexer part (Id.) (Cairns2, Fig. 12, column 10, lines 18-41) (Nitta, Fig. 2, column 3, lines 23-33; column 4, lines 35-30).

108. **As for claim 16,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the holding part comprises:

109. positive path capacitors charging and holding the positive pixel signals from the positive path switches of the second demultiplexer (Cairns2, Fig. 3, item 25) part; and

110. negative path capacitors charging and holding the negative pixel signals from the negative path switches of the second demultiplexer (Id.) part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

111. **As for claim 17,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the discharging part comprises:

112. a second multiplexer part (Cairns1, Fig. 4, item 14) having:

113. a plurality of positive path switches connected to the positive path switches of the second demultiplexer (Cairns1, Fig. 4, item 14) through the holding part and connected to the data lines; and

114. a plurality of negative path switches connected to the negative switches of the second demultiplexer (Id.) through the holding part and connected to the data lines (column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}).

115. **As for claim 18,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer, the demultiplexer (Cairns2, Fig. 3, item 25), and the second demultiplexer (Id.) are controlled by a first control signal through an input polarity control signal and an ODD/EVEN signal performing the time-division on a horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

116. **As for claim 19,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the ODD/EVEN signal performsthe time-division on an enable period determined by a source output enable signal for the horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

117. **As for claim 20,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the ODD/EVEN signal further performs the time-division on a disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

118. **As for claim 21,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer part, the demultiplexer (14) part in Fig.4 and section [0015] {Cairns1} and in

column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}. The combination of Cairns2 and Nitta teaches that the second demultiplexer (64) part recharge the holding part with the pixel signals for the disable period, wherein the pixel signals are generated for a previous enable period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

119. **As for claim 22,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the source output enable signal is generated by increasing the disable period of an external reference source output enable signal in order to secure a recharging period of the holding part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

120. **As for claim 23,** Cairns1 as modified by Cairns2, Enami and Nitta teaches the second multiplexer part is controlled by the first control signal and a second control signal that is phase-inversed with respect to the first control signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

121. **As for claim 24,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that an output buffer (Cairns2, Fig. 11b, item 40) part buffering the pixel signals discharged from the holding part to the discharging part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

122. **As for claim 25,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part comprises: a plurality of positive path output buffers (Id.) connected between the positive path capacitors of the holding part and the positive path switches of the second multiplexer part; and a plurality of negative path output buffers (Id.) connected between the negative path capacitors of the holding part and the negative path switches of the second multiplexer part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

123. As for claim 26, Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part buffering the pixel signal supplied through the output channels of the second multiplexer part and supplying the pixel signals to each of the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

124. **As for claim 27,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part comprises: a plurality of output buffers (Cairns2, Fig. 11b, item 40) connected between the output channels of the second multiplexer part and the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

125. **As for claim 29,** Cairns1 as modified by Cairns2, Enami and Nitta teaches of: teaches that a third multiplexer part supplying the pixel signals from the output part to the corresponding

data lines for the enable period of the source output enable signal and commonly supplying a reference voltage of the liquid crystal cells to the corresponding data lines for the disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

Conclusion

126. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

127. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

128. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

129. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

130. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
8 January 2009

Tammy Pham
/Tammy Pham/
Examiner, Art Unit 2629